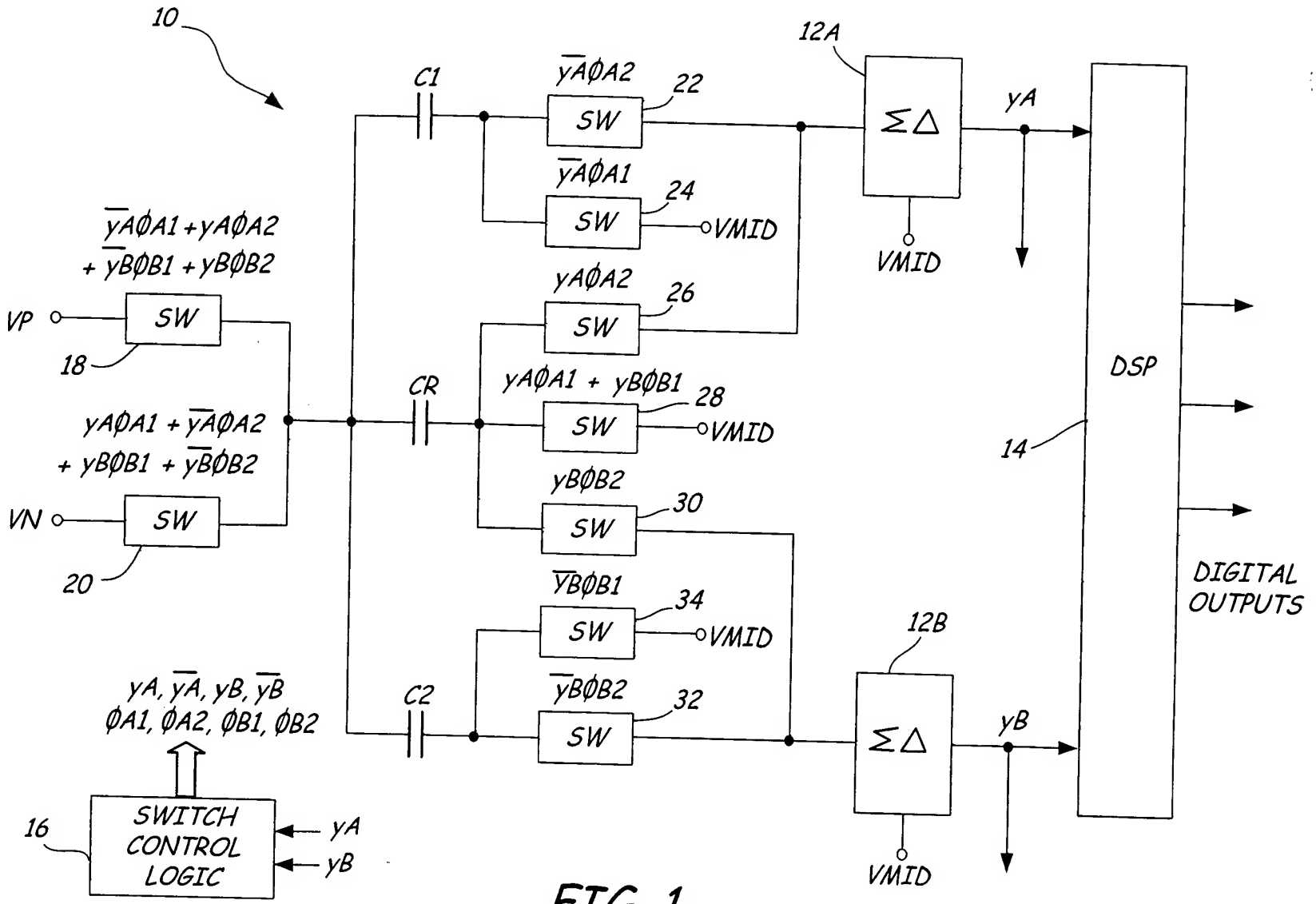
10
C1
$\overline{yA}\phi A2$
22
SW
12A
$\Sigma\Delta$
yA
$\overline{yA}\phi A1$
24
SW
VMID
VMID
$\overline{yA}\phi A1 + yA\phi A2$
$+ \overline{yB}\phi B1 + yB\phi B2$
VP
SW
18
$yA\phi A2$
26
SW
CR
$yA\phi A1 + yB\phi B1$
28
SW
VMID
DSP
14
$yA\phi A1 + \overline{yA}\phi A2$
$+ yB\phi B1 + \overline{yB}\phi B2$
VN
SW
20
$yB\phi B2$
30
SW
$\overline{yB}\phi B1$
34
SW
VMID
12B
$yA, \overline{yA}, yB, \overline{yB}$
$\phi A1, \phi A2, \phi B1, \phi B2$
C2
$\overline{yB}\phi B2$
32
SW
$\Sigma\Delta$
yB
DIGITAL
OUTPUTS
16
SWITCH
CONTROL
LOGIC
yA
yB
VMID

FIG. 1

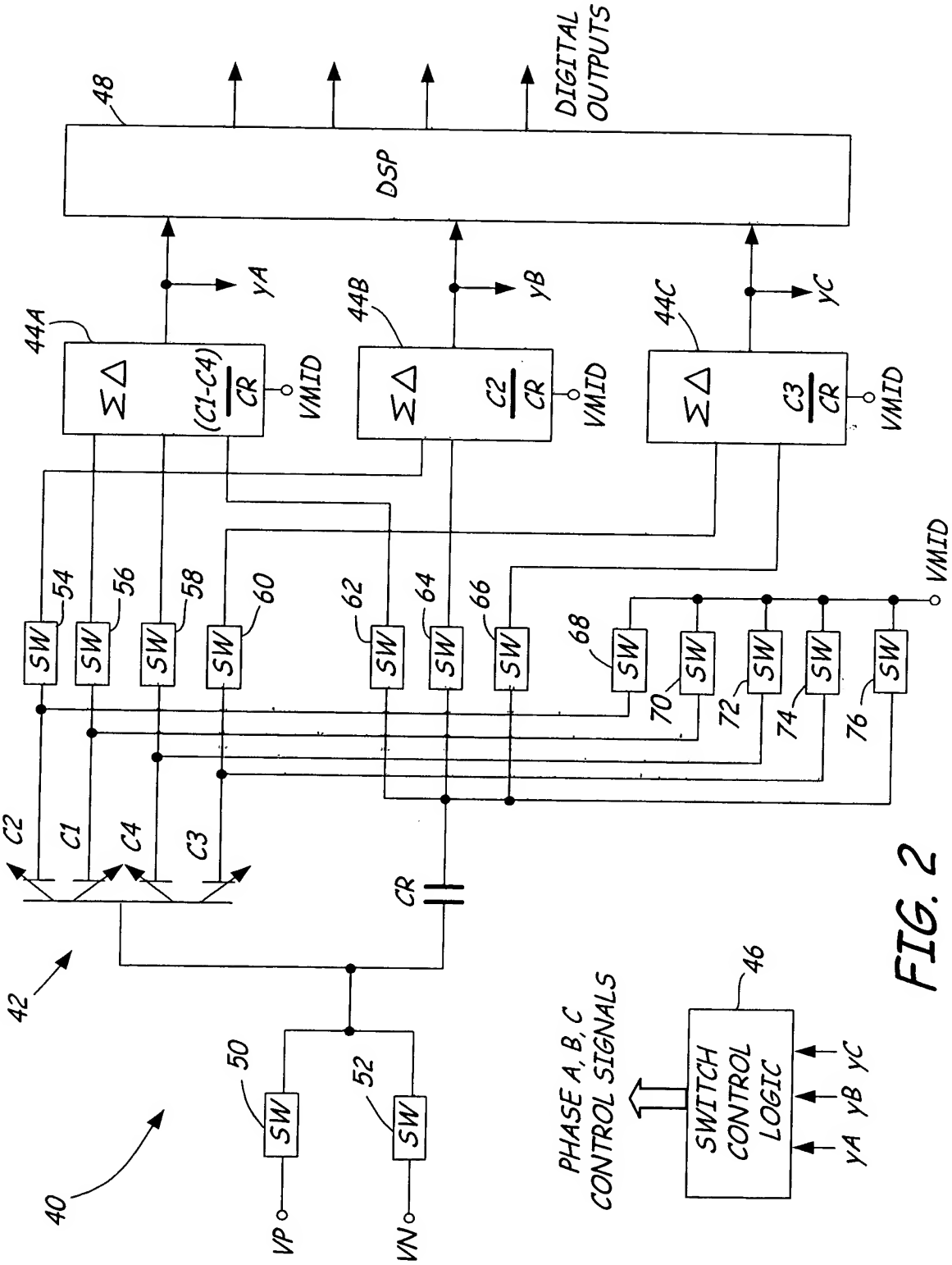
DIGITAL OUTPUTS
48
DSP
YA
YB
YC
44A
44B
44C
ΣΔ
(C1-C4)/CR
C2/CR
C3/CR
VMID
54
56
58
60
62
64
66
68
70
72
74
76
SW
C2
C1
C4
C3
CR
42
40
50
52
VP
VN
PHASE A, B, C CONTROL SIGNALS
46
SWITCH CONTROL LOGIC

FIG. 2